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| APPLICATION NO.                     | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|-------------------------------------|-------------|----------------------|---------------------|------------------|
| 10/708,715                          | 03/19/2004  | Karen A. Bard        | BUR920030172US1     | 2714             |
| 23550                               | 7590        | 12/20/2005           | EXAMINER            |                  |
| HOFFMAN WARNICK & D'ALESSANDRO, LLC |             |                      | LIN, SUN J          |                  |
| 75 STATE STREET                     |             |                      | ART UNIT            |                  |
| 14TH FL                             |             |                      | PAPER NUMBER        |                  |
| ALBANY, NY 12207                    |             |                      | 2825                |                  |

DATE MAILED: 12/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/708,715

Applicant(s)

BARD ET AL.

Examiner

Sun J. Lin

Art Unit

2825

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 19 March 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-3, 6-10, 13-15, 19 and 20 is/are rejected.
- 7) ☒ Claim(s) 4, 5, 11, 12 and 16-18 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 19 March 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>03/19/04</u> . | 6) <input type="checkbox"/> Other: _____  |

### DETAILED ACTION

1. This office action is in response to application 10/708,715 filed on 03/19/2004. Claims 1 – 20 remain pending in the application.

#### *Claim Objections*

2. Claims listed below are objected to because of the following informalities:

Claim 1, line 2, before “steps” delete ~~the~~.

Claim 2, line 1, change “the step” to ~~a step~~.

Claim 3, line 1, change “the step” to ~~a step~~.

Claim 4, line 1, change “the step” to ~~a step~~.

Claim 5, line 1, change “the step” to ~~a step~~.

Claim 5, line 2, before “modification” delete ~~the~~.

Claim 5, line 2, delete ~~is required~~.

Claim 5, line 3, after “design” insert ~~is required~~.

Claim 5, line 3, after “modification” insert ~~of the edge of the failing FET~~.

Claim 6, line 2, before “FET edge” insert ~~failing~~.

Claim 8, line 2, change “method” to ~~system~~.

Claim 8, line 2, delete ~~the steps of~~.

Claim 12, line 2, before “modification” delete ~~the~~.

Claim 12, line 2, delete ~~is required~~.

Claim 12, line 3, after “design” insert ~~is required~~.

Claim 12, line 3, after “modification” insert ~~of the edge of the failing FET~~.

Claim 16, line 7, before “modification” delete ~~the~~.

Claim 16, line 8, delete ~~is required~~.

Claim 16, line 8, after “design” insert ~~is required~~.

Claim 16, line 8, after “modification” insert ~~of the edge of the failing FET~~.

Appropriate correction is required.

#### *Claim Rejections - 35 USC § 103*

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

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(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

- (1). Determining the scope and contents of the prior art.
- (2). Ascertaining the differences between the prior art and the claims at issue.
- (3). Resolving the level of ordinary skill in the pertinent art.
- (4). Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 1 – 3, 6 – 10, 13 – 15, 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over *applicants' admitted prior art* (called AAPA hereinafter) in view of technical Presentation view graphs entitled “*BSIM4 Model and Parameter Extraction*” prepared by Assenmacher over U.S. Patent Application Publication No. 2003/0182640 A1 to Alani et al.

5. As to Claim 1, AAPA (Paragraph 0004 – 0007] discloses the following subject matter:

- Using computer-based tool (e.g., signal integrity analyzer) to conduct a signal integrity analysis on an IC (e.g., CMOS) design – [Paragraph 0006]; A signal integrity analyzer (i.e., tool) can provide an indication of signal integrity failure of an IC design when it fails signal integrity analysis – [Paragraph 0006].
- For a component (e.g., FET) in an IC design, sensitivity to electrical noise is determined by its threshold voltage  $V_t$  – [Paragraph 0005]; Threshold voltage  $V_t$  of a component (FET) in an IC design may be shifted to an undesired level due to its active area is being too close to a well edge – [Paragraph 0004].

AAPA does not disclose a method of identifying any FET in an IC design that may cause a signal integrity failure. But Assenmacher teaches a method of using parameterized SPICE well proximity macro (FET) models using distances of devices (i.e., FET's) to well edges as instance parameters in evaluation of threshold voltage  $V_t$

degradation of devices (FET's) in an IC design – [Page 18]. Assenmacher also discloses the following subject matter:

- Well proximity effect is a manufacturing technology issue and layout dependent effects – [Page 18]; Well proximity effect is dependent upon (1) device orientation (2) distance of well edge to active area of device; Notice that (1) the device is a FET component in an IC design (2) the well proximity effect is dependent upon closeness of locations of FET's relative to well edges, which is dependent upon layout of FET's in an IC design.

Assenmacher teaches using SPICE tool in evaluation of well proximity effect of FET components in an IC design; he does not disclose a method of utilizing SPICE tool in performing signal integrity analysis of the IC design. But Alani et al. teach implementation of SPICE tool in a signal integrity analysis system (SIAS) tool for use in performing signal integrity analysis of a pre-defined circuit layout (e.g., IC layout) – [abstract; Fig. 1; Fig. 3]. Alani et al. also disclose in Fig. 1 that a 3<sup>rd</sup> party SPICES tool (e.g., SPICE well proximity macro models) can be interfaced with the SIAS for use in performing signal integrity analysis of a pre-defined circuit layout. Alani et al. also disclose the following subject matter:

- Repeat running signal integrity analysis simulation 314 after updating parameters (e.g., distances between FET edge and a well edge) of a SPICE tool (e.g., tool using SPICE well proximity macro models) – [Fig. 3];
- Simulation predefined circuit layout from SPICE netlist – [abstract]; netlist extraction – [Fig. 1]; Notice that a SPICE netlist defines locations of all components (i.e., FET's) of a circuit layout.

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have applied the teachings of Assenmacher and Alani et al. in implementing the SPICE well proximity macro models in the SIAS tool in order to conducting signal integrity analysis of an IC design and to identifying locations of all FET's that have active areas too close to well edges in case that the IC design fails the signal integrity analysis, which is indicated by the SIAS tool.

Notice that Assenmacher discloses in a drawing on page 18 and indicates that the well proximity effect, which is a layout dependent effect, is dependent upon *distance* between an edge of a FET and a well edge. Notice that, according to well proximity effect model, when spacing between an edge of a FET and a well edge closer than a distance (called threshold distance) the degradation of signal integrity becomes severe. Therefore, in order to eliminate signal integrity failure, a FET having an edge that is closer than the threshold distance to a well edge should be modified (e.g., increasing the distance between a failing FET edge and a nearby well edge).

For reference purposes, the explanations given above in response to Claim 1 are called [Response A] hereinafter.

6. As to Claims 8 and 15, reasons are included in [Response A] given above.
7. As to Claims 2, 3, 9 and 10, reasons are included in [Response A] given above. Notice that the step of repeating is illustrated in a looping around steps 320 – 314 – 318 – 320 in Fig. 3.
8. As to Claims 6, 13 and 19 reasons are included in [Response A] given above.
9. As to Claims 7, 14 and 20 reasons are included in [Response A] given above.

***Allowable Subject Matter***

10. Claims 4, 5, 11, 12, 16, 17 and 18 are objected to as being dependent upon a rejected base claim, but they would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Those claims are allowed is because that the prior art does not teach or fairly suggest the following subject matter:

- A method of designing an integrated circuit for signal integrity comprises a step of reporting that a signal integrity failure cannot be corrected by modification of an edge of any failing FET in the case that all failing FET edges have been modified in combination with other limitations as recited in **Claim 4**;
- A method of designing an integrated circuit for signal integrity comprises a step of reporting that the modification is required to a physical IC design in the case that the modification an edge of a failing FET corrected an identified signal integrity failure in combination with other limitations as recited in **Claim 5**;
- A system of designing an integrated circuit for signal integrity comprises means for reporting that a signal integrity failure cannot be corrected by modification of an edge of any failing FET in the case that all failing FET edges have been modified in combination with other limitations as recited in **Claim 11**;
- A system of designing an integrated circuit for signal integrity comprises means for reporting that the modification is required to a physical IC design in the case that the modification of an edge of a failing FET corrected an identified signal integrity failure in combination with other limitations as recited in **Claim 12**;
- A computer program for designing an integrated circuit for signal integrity comprises program code configured to report that the modification is required to a physical IC design in the case that the modification an edge of a failing FET corrected an identified signal integrity failure in combination with other limitations as recited in **Claim 16**.

### **Conclusion**

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sun J Lin whose telephone number is (571) 272 - 1899. The examiner can normally be reached on Monday-Friday 9:30AM - 6:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S Smith can be reached on (571) 272 - 1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sun James Lin  
Patent Examiner  
Art Unit 2825  
December 7, 2005

A handwritten signature in black ink, appearing to read "James Lin", is positioned to the right of the typed name and date.